

REMARKS

I. Status of the Claims

Claims 27, 28, and 30-34 are currently pending in this application. Applicants add claim 34 to define further aspects of their invention. Support for new claim 34 can be found in the specification in, for example, Figures 12H and 13D.

II. Rejections Under 35 U.S.C. § 102(b)

The Examiner rejected claims 27, 28, and 30 - 33 under 35 U.S.C. § 102(b), as being anticipated by U.S. Patent No. 4,445,267 ("De La Moneda et al.") for reasons discussed at pages 2-4 of the Office Action. Applicants respectfully traverse the Examiner's rejection for the following reasons.

A rejection under § 102 is proper only when the claimed subject matter is identically described or disclosed in the prior art. *In re Arkley*, 455 F.2d 586, 587 (C.C.P.A. 1972). "For anticipation under 35 U.S.C. § 102, the reference must teach every aspect of the claimed invention either explicitly or impliedly." M.P.E.P. § 706.02.

De La Moneda et al. does not anticipate the pending claims, because the reference fails to teach each and every element of the claims. Specifically, De La Moneda et al. at least fails to teach the claimed "a side wall of the first gate electrode is connected to a side wall of the second gate electrode above the isolation element when viewed from a direction perpendicular to the first direction," as recited in independent claim 27.

In the Office Action, the Examiner asserts that De La Moneda et al. teaches a semiconductor device in which a side wall of a first gate electrode 20 of a first transistor is connected to a side wall of a second gate electrode 20 of a second transistor above

an isolation element. See Office Action at 3. The Examiner further indicated that Figure 10 of De La Moneda et al. shows a conductive layer 42 “connecting over isolation element 12.” See Office Action at 3.

Applicants respectfully disagree with the Examiner’s allegations. De La Moneda et al. teaches a semiconductor device in which the side walls of adjacent gate electrodes 20 are covered by insulating silicon dioxide layers 38. See col. 7, lines 12-17. See also, Figure 10 of De La Moneda et al. Although the conductive layer 42 appears to connect the transistor devices in De La Moneda et al., layer 42 does not connect the side walls of the adjacent gate electrodes 20. In fact, insulating layers 38 cover the side walls of gate electrodes 20 such that these gate electrodes are not connected to each other physically or electrically. Therefore, De La Moneda et al. does not teach, at least, “a side wall of the first gate electrode is connected to a side wall of the second gate electrode above the isolation element when viewed from a direction perpendicular to the first direction,” as recited in claim 27.

In light of the above-described deficiencies of De La Moneda et al., Applicants respectfully submit that claim 27 is allowable over the applied reference. Moreover, claims 28, and 30-34 are allowable at least due to their dependence from claim 27.

Please grant any extensions of time required to enter this response and charge
any additional required fees to our deposit account 06-0916.

Respectfully submitted,

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